Single-Phase Energy Metering Chip with Built-in Calibration Function

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Abstract

This paper presents a single-phase energy metering chip with built-in calibration function to measure electric power quantities. The entire chip consists of an analog front end, a filter block, a computation engine, a calibration engine, and an external interface block. The key design issues are how to reduce the implementation costs of the computation engine from repeatedly used arithmetic operations and how to simplify calibration procedure and reduce calibration time. The proposed energy metering chip simplifies the computation engine using time-division multiplexed arithmetic units. It also provides a simple and fast calibration scheme by using integrated digital calibration functionality. The chip is fabricated with 0.18-μm six-layer metal CMOS process and housed in a 32-pin quad-flat no-leads (QFN) package. It operates at a clock speed of 4096 kHz and consumes 9.84 mW in 3.3 V supply.

Keywords: energy meter, analog front end, computation engine, calibration, SoC

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1. Introduction

As the energy consumption in a household continues to increase, the need to precisely measure and control alternating current (AC) power has increased. Recently, energy metering technology has been applied to various smart home devices and appliances in order to monitor and control energy usage [1]. An energy metering chip measures 110 V or 220 V AC voltage and current applied to a load, and it calculates the corresponding power consumption and energy. In addition, it also monitors a variety of conditions, such voltage sag or swell, over-current and so on.

The energy metering chip is interface to both voltage and current sensing elements. A resistor divider is widely used as the voltage sensor. A low resistance shunt or a current transformer (CT) is commonly used as the current sensor. The current shunt offers good accuracy at low cost, and the measurement is simple. However, its parasitic inductance and self-heating problem makes it unsuitable for large current measurement [2, 3]. The CT can measure up to very high current and consumes little power. However, it typically has a small phase shift of between 0.1° and 0.3° because of the magnetizing current [3]. These sensing elements and an associated RC interface circuits affect the magnitude and phase of the sensed signals, and results in the degradation of measurement accuracy. In addition, component tolerances, residual analog-to-digital converter (ADC) offset, and system noise also degrade the performance. Therefore, the various system calibrations, such as offset correction, phase calibration, and gain calibration, are required for precise measurements.

The energy metering chip can be implemented with a microcontroller or in hardwired logic. The microcontroller-based implementation of the energy metering chip is easier and faster compared to the fully hardwired implementation. The ease of addition and modification of functionality through embedded S/W upgrade is another advantage of the microcontroller-based implementation, making it suitable for various applications. However, the power consumption and implementation costs of the microcontroller-based solution are known to be higher than its hardwired counterpart. Depending on the type of application, the energy metering chip needs to operate non-stop for long hours, making low-energy consumption essential. In addition, systems using the energy metering chip require system calibration for accurate energy measurement. The chip's system calibration is a time consuming and complicated process which affects mass production. Therefore, an effective system calibration method is necessary.

There are several issues in the design and implementation of the fully hardwired energy metering chip. First, the arithmetic operations such as multiplication and division are repeatedly used to calculate the electric power quantities, which complicate the chip's computation block and increase hardware (H/W) implementation costs. Therefore, an efficient architecture is required to simplify the computation block using time-division multiplexed arithmetic units. Second, an accurate source is commonly required for the system calibrations to be performed accurately. The source generates any desired voltage, current, and phase shifts between the voltage and current. However, it is usually expensive and is not easily available. Calibration method using only a purely resistive load can provide simplicity and convenience, although it has less accuracy compared with that using an accurate source. Last, the system calibrations are normally performed with a personal computer (PC) based calibration controller. The calibration parameters such as the gain, offset, and phase are calculated in the

calibration controller and are delivered to the energy metering chip. This method increases calibration time and complicates calibration procedure. Hence, a built-in calibration function is required for a simple and fast calibration.

In this paper, an efficient energy metering chip architecture to achieve low H/W complexity as well as simple and fast calibration is proposed. The remainder of this paper is organized as follows. The system overview and power definitions are described in Section 2, and the computation engine architecture and the calibration scheme are described in Section 3. Implementation results and conclusions are given in Sections 4 and 5, respectively.

2. System Description

In this section, a brief description of a single-phase energy meter is given and power definitions are described in order to understand the architecture and calibration scheme proposed. In **Table 1**, the list of symbols and definitions used across the paper is presented for reference purposes.

The single-phase energy meter is composed of a voltage sensor, a current sensor, an energy metering chip, and a micro-controller as shown in **Fig. 1**. The AC voltage and current applied to the load are input to the energy metering chip through the sensing elements. The chip converts the analog signals to digital samples, and then performs the process of calculating the root mean square (RMS) and power using the sensed samples. It also stores the calculated RMS and power measurements into the registers and communicates with the external micro-controller via the external interface block.

The IEEE standard 1459 shows some definitions to measure electric power quantities in a single-phase system under sinusoidal condition [4]. The instantaneous voltage and current can be expressed as shown in (1) and (2), respectively.

$$v(t) = \sqrt{2}V \sin \omega t \tag{1}$$

$$i(t) = \sqrt{2}I \sin(\omega t - \theta) \tag{2}$$

where V and I are the RMS values of the voltage and current signals, respectively. ω is the angular frequency $2\pi f_L$, f_L is the line frequency, e.g. 50 or 60 Hz, and θ is the phase angle between the current and voltage signals and t is the time.

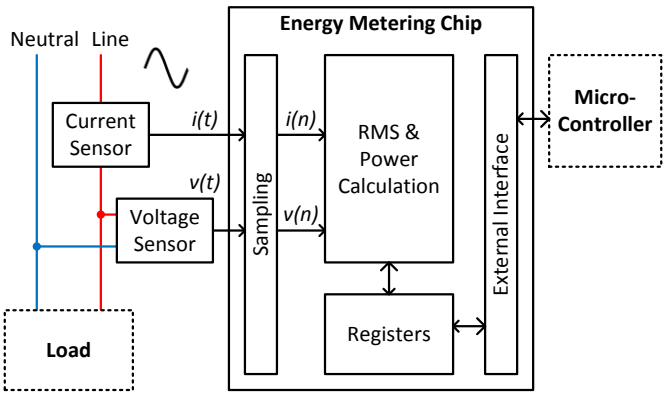

Fig. 1. Single-phase energy meter

Table 1. Symbols and definitions

Symbol	Description
P	Active power
Q	Reactive power
S	Apparent power
PF	Power factor
V_{RMS}	Voltage RMS
$v(t)$	Instantaneous voltage
$i(t)$	Instantaneous current
$f_L(i)$	i-th measured line frequency
$\theta(i)$	i-th phase difference between voltage and current
$\Delta d(i)$	i-th delay difference between voltage and current
$d_V(i)$	i-th calibrating delay for voltage channel
$d_I(i)$	i-th calibrating delay for current channel
$e_{VRMS}(i)$	Voltage RMS error
$g_V(i)$	i-th calibrating gain for voltage channel
$v_\varphi(t)$	Output of variable phase shifter
$H_S(z)$	Transfer function of $\pi/2$ phase shifter
$e_{\%}$	Relative error

The active power is the average value of the instantaneous power which is the product of the instantaneous voltage and the instantaneous current during the observation time interval from τ to $\tau+kT$, and it is given by

$$P = \frac{1}{kT}\int_{\tau}^{\tau+kT} v(i)\cdot i(t)dt = VI\cos\theta \tag{3}$$

where τ is the moment when the time starts, k is a positive integer number, and $T=1/f_L$ is the line cycle time.

The reactive power is the average value of the instantaneous reactive power which is obtained by multiplying the instantaneous current by the instantaneous quadrature voltage. The instantaneous quadrature voltage is obtained by phase shifting instantaneous voltage $\pi/2$ using an integrator with ω gain. The reactive power is defined by

$$Q = \frac{1}{kT}\int_{\tau}^{\tau+kT} i(t)\cdot\left[\omega\int v(t)dt\right]dt = VI\sin\theta \tag{4}$$

The apparent power is defined as the maximum power that can be delivered to a load, and it is the product of the RMS voltage and the RMS current as shown in (5).

$$S = VI = \sqrt{P^2 + Q^2} \tag{5}$$

The power factor is the ratio between the energy transmitted to the load over the maximum energy. It is defined as the active power divided by the apparent power as shown in (6).

$$PF = \frac{P}{S} = \cos\theta \tag{6}$$

The RMS value of the voltage is defined as shown in (7), and the RMS value of the current is obtained by (7).

$$V_{RMS} = \sqrt{\frac{1}{kT}\int_{\tau}^{\tau+kT} v^2(t)dt} = V \tag{7}$$

3. Energy Metering Chip Architecture

In this section, the proposed energy metering chip architecture is described. A brief description of the architecture is given, and a computation engine architecture and a calibration scheme are proposed.

Fig. 2 shows the block diagram of the proposed energy metering chip. It includes an analog front end (AFE), a filter block, a computation engine (CE), a calibration engine (CAL), internal registers, and an external interface block. The AFE incorporates two programmable gain amplifiers (PGAs) and two third-order ΣΔ modulators. The PGAs are interface to the voltage and current sensors and independently amplify the sensed voltage and current, respectively. Both ΣΔ modulators simultaneously convert the analog voltage and current signals to single-bit digital data streams, and sample at a rate of 1024 kHz. The ΣΔ modulator is implemented using a cascaded integrator feed-forward (CIFF) architecture.

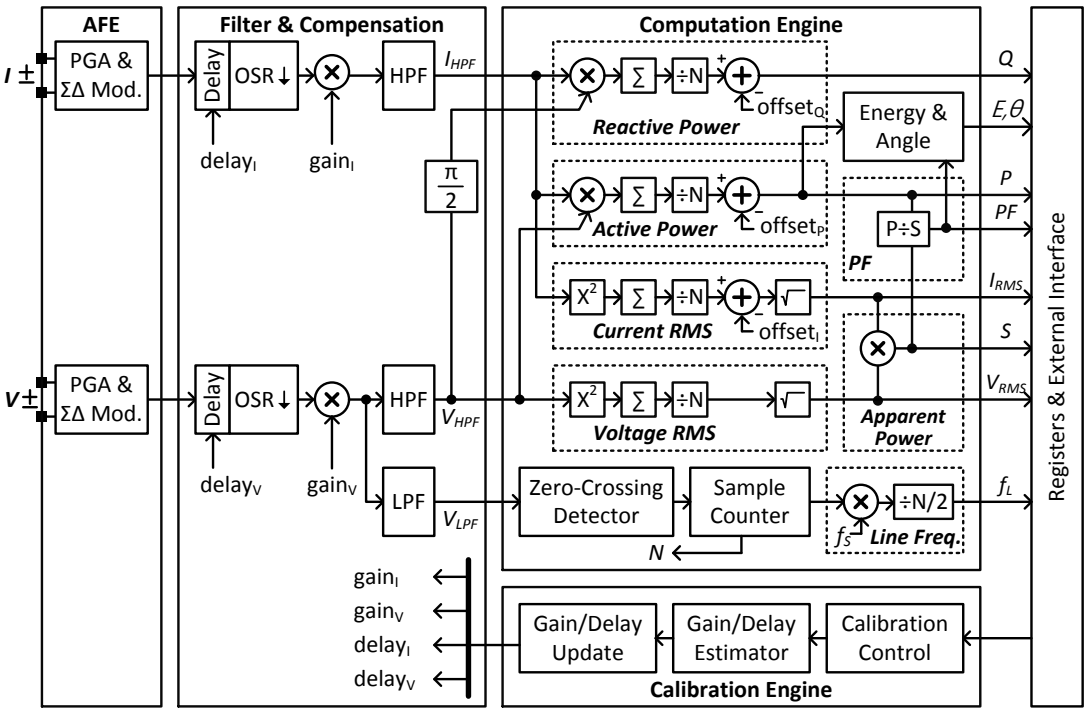

Fig. 2. Block diagram of energy metering chip

The filter block consists of two decimation filters, two high-pass filters (HPFs), and a low-pass filter (LPF). The single-bit ΣΔ modulator output data streams are widened to 24-bit words and down-sampled to 8 kHz with both decimation filters. The decimation filter includes a fourth-order cascaded integrator-comb (CIC) filter and a compensation filter. The CIC filter is widely used as the decimation filter because it requires no multiplication or coefficient storage but rather only additions and subtractions [5]. The CIC and compensation filters are used to achieve sampling rate decrease and compensate for the amplitude roll-off of the CIC filter, respectively. The compensation filter is implemented using a finite impulse response (FIR) filter. Both HPFs remove any DC component from the voltage and current signals. The LPF removes noise and harmonic components included in the voltage signal, and it results in a stable and accurate frequency measurement tolerant of noise and harmonics. The HPF and LPF are implemented using first-order infinite impulse response (IIR) filters with a cutoff frequency of 4.45 Hz and 140 Hz, respectively.

The CE performs power measurements, line-voltage period measurement, and RMS calculation on the voltage and current. The CAL performs the precise estimate of errors in the gain and phase of the sensed voltage and current signals. The measured values generated from the CE are stored in registers. The external interface block communicates with the external micro-controller via such as an Inter-Integrated Circuit (I2C), a universal asynchronous receiver/transmitter (UART), or a Serial Peripheral Interface (SPI).

3.1 Computation Engine

From (7), the RMS value of the voltage or current signal is calculated by squaring the signal, taking the average, and obtaining the square root. The integration in continuous time is equivalent to the discrete time accumulation or summation. Therefore, the RMS calculation requires four arithmetic operations such as multiplication, accumulation, division, and square root operation. Arithmetic operations for the active, reactive, and apparent powers and the power factor can be obtained from (3) to (6), respectively. A line frequency measurement based on the zero-crossing detection of the voltage signal is given by

$$f_L(i) = \frac{f_S \cdot N_{ZC}(i)}{2N(i)} \tag{8}$$

where i is the measurement count, f_S is the sampling frequency, $N_{ZC}(i)$ is the number of zero-crossings for the voltage signal, and $N(i)$ is the sample count during the zero-crossing detection. The line frequency measurement requires a multiplication and a division since $2N(i)$ is obtained by shifting 1-bit to the left. The arithmetic operations for the CE require six multiplications, four accumulations, six divisions, and two square roots, as shown in **Table 2**.

The proposed CE architecture using time-division multiplexed arithmetic units is shown in **Fig. 3**. It requires two multipliers, four accumulators, a divider, a square root block, seven multiplexers (MUXs), and temporary registers. The two multipliers, the divider, and the square root block are time-division multiplexed to perform RMS and power calculations. The values generated from one of the arithmetic units are temporarily stored in registers, and then are used in the other arithmetic unit.

The proposed CE operates as follows. An instantaneous voltage, an instantaneous current, and an instantaneous quadrature voltage are sequentially input to the multiplier1 through two MUXs every sampling clock. The multiplier1 sequentially calculates four values: squared voltage, squared current, instantaneous active power, and instantaneous reactive power. These

four values are independently accumulated in four accumulators during the averaging duration which is the sample count $N(i)$ divided by the sampling frequency f_S, and then four accumulated samples are sequentially input to the divider once every averaging period. All accumulators are reset when the new averaging operation begins. The divider generates an averaged squared voltage, an averaged squared current, active power, and reactive power using the output of all accumulators and the sample count $N(i)$ generated from the sample and zero-crossing counter. The square root block generates the RMS values of the voltage and current using the output of the divider. The multiplier2 generates the apparent power using the output of the square root block. The divider generates the power factor using the active power stored in the register and the output of the multiplier2. It also generates a temporary value $N_{ZC}(i)/N(i)$ for line frequency. The multiplier2 generates the line frequency.

For low H/W implementation costs, the multiplier, the divider, and the square root block are implemented using a shift-and-add multiplication algorithm, a non-restoring division algorithm, and a non-restoring square root algorithm, respectively [6]-[11]. The conventional CE using individual arithmetic units requires six multipliers, four accumulators, six dividers, and two square roots, whereas the proposed CE requires two multipliers, four accumulators, a divider, a square root block, seven multiplexers (MUXs), and temporary registers. The implementation result shows 33.99 % reduction in equivalent gate count compared with the conventional CE. Details of the result are given in **Table 3**.

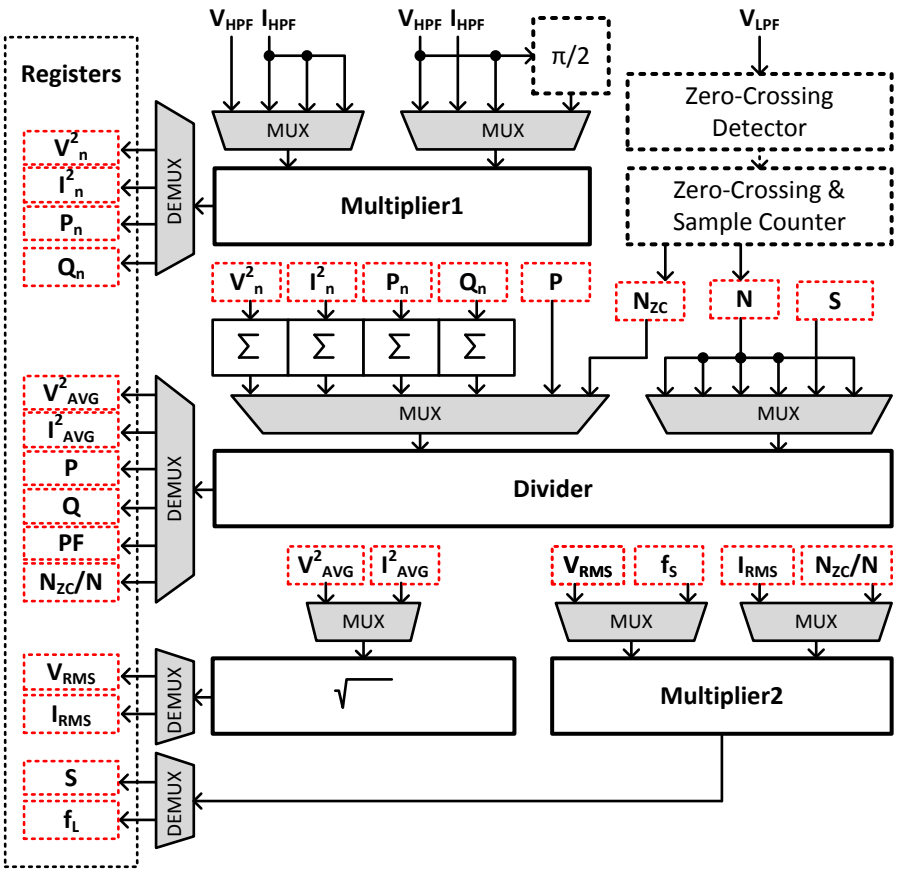

Fig. 3. Computation engine architecture

Table 2. Arithmetic operation for computation engine

Calculation	Multiplication	Accumulation	Division	Square Root
Voltage RMS	1	1	1	1
Current RMS	1	1	1	1
Active Power	1	1	1	0
Reactive Power	1	1	1	0
Apparent Power	1	0	0	0
Power Factor	0	0	1	0
Line Frequency	1	0	1	0
Total	6	4	6	2

Table 3. Comparison of conventional and proposed computation engine

Function Blocks	Proposed		Conventional	
	Num.	Gate[1]	Num.	Gate
24-bit x 24-bit multiplier	1	1,594	4	6,376
64-bit Accumulator	4	3,248	4	3,248
74-bit x 32-bit divider	1	1,931	6	11,586
32-bit x 32-bit multiplier	1	2,185	2	4,370
32-bit square root	1	1,930	2	3,860
Zero-crossing & Counter	1	1,258	1	1,258
Temporary registers	1	3,269	0	0
MUXs & etc.	1	4,849	0	0
Total gate count		20,264		30,698

[1]Gate refers to a 2-input NAND gate

3.2 Calibration Engine

A power factor is commonly used to calibrate the phase shift caused by a current sensor since it is equal to the cosine of the phase angle between the voltage and current under sinusoidal condition. The power factor is insensitive to phase changes at high power factor. Therefore, if the phase calibration is performed at a power factor of 1, the accuracy may degrade more compared to that performed at a power factor of 0.5. For example, a power factor error of 0.1% results in phase error of 2.5626˚ at a power factor of almost 1 because $\cos^{-1}(0.999)$ is equal to 2.5626˚, whereas the phase error is equal to 0.0661˚, that is $\cos^{-1}(0.499)$, at a power factor of 0.5. However, there may be more power factor errors at low power compared to that at high power factor, since the value of the active power is small at low power factor. For this reason, the phase calibration is usually performed at a power factor of 0.5 with an accurate source that is able to generate any desired voltage, current, and phase shifts between the voltage and current.

The proposed calibration scheme can be performed with a purely resistive load at a power factor of 1. **Fig. 4** shows the proposed calibration scheme. It requires an additional variable phase shifter to change phase shifts between the voltage and current. The CAL calculates the calibrating gains and delays for both voltage and current channels using the measured values generated from the CE. The calibrating gains and delays are used to compensate both the voltage and current signals.

The proposed phase calibration procedure is as follows. First, the variable phase shifter is used to set the phase of the instantaneous voltage to φ degree, e.g. 60˚. After CE operation, a measured power factor and a measured line frequency are stored in the register. The CAL estimates the phase difference between the voltage and current and calculates the

corresponding delay using the measured power factor and the measured line frequency as shown in (9) and (10), respectively.

$$\theta(i) = \cos^{-1}\left(PF(i)\right) - \varphi \tag{9}$$

$$\Delta d(i) = \frac{f_{AFE}}{f_L(i)} \frac{\theta(i)}{360°} \tag{10}$$

where i is an iteration count, $PF(i)$ is the i-th measured power factor, φ is the phase shift generated by the variable phase shifter, $f_L(i)$ is the i-th measured line frequency, and f_{AFE} is the sampling frequency used for the AFE, i.e. 1024 kHz. If the absolute value of the estimated phase is greater than the predefined tolerance value and the iteration count is less than the predefined maximum iteration value, the iteration count is increased by one. And if the estimated phase is a positive value, the calibrating delay for the voltage channel is updated. Otherwise, the calibrating delay for the current channel is updated. Both delays are updated as follows:

$$d_V(i+1) = d_V(i) + \Delta d(i) \cdot sign\{\theta(i)\} \tag{11}$$

$$d_I(i+1) = d_I(i) + \Delta d(i) \cdot sign\{-\theta(i)\} \tag{12}$$

where initial delays, $d_V(0)$ and $d_I(0)$, are equal to 0 or the last calibrating delays. Then, the calibration procedure is performed repeatedly until the absolute value of the estimated phase is less than the tolerance value or the iteration count is equal to the predefined maximum iteration value.

The gain calibration is similar to the phase calibration. After CE operation, the measured voltage RMS is stored in the register. The CAL estimates the voltage RMS error and calculates the calibrating gain as shown in (13) and (14), respectively.

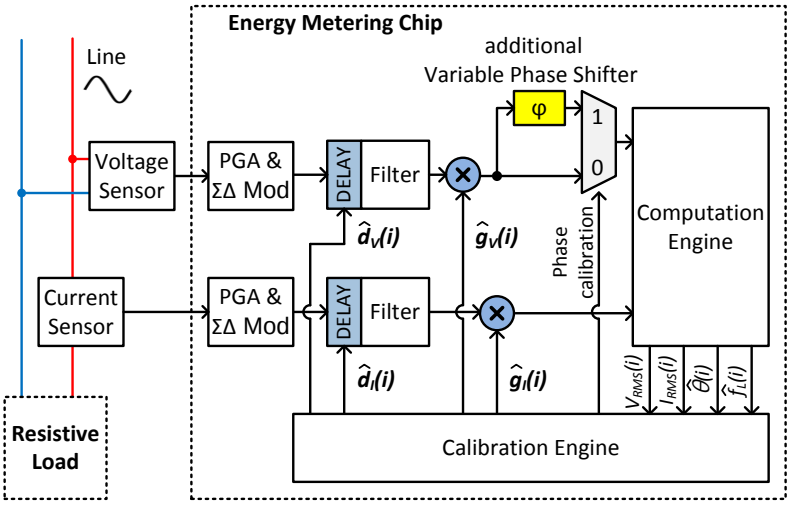

Fig. 4. Gain and phase calibration scheme

$$e_{VRMS}(i) = \left| V_{RMS}(i) - V_{REF} \right| \tag{13}$$

$$g_V(i+1) = g_V(i) \cdot \frac{V_{REF}}{V_{RMS}(i)} \tag{14}$$

where V_{REF} is the expected RMS value, and $V_{RMS}(i)$ is the i-th measured voltage RMS value. An initial gain $g_V(0)$ is equal to 1 or the last calibrating gain. The gain calibration procedure is performed repeatedly until the estimated error is less than the tolerance value or the iteration count is equal to the predefined maximum iteration value. The current gain calibration is simultaneously performed with the same method of the gain calibration.

The output of the variable phase shifter is obtained by

$$v_\varphi(t) = v(t) \cdot \cos\varphi + 2\pi f_L \int v(t)dt \cdot \sin\varphi \tag{15}$$

where $v(t)$ is $sin(\omega t)$, φ is the phase shift generated by the variable phase shifter, f_L is the line frequency, and t is the time. The variable phase shifter includes two multipliers, an adder, and a $\pi/2$ phase shifter as shown in **Fig. 5**. The $\pi/2$ phase shifter is implemented using the Simpson integrator as shown in **Fig. 6** and its transfer function is given by (16) [12], [13].

$$H_S(z) = \frac{2\pi f_L(i)}{3 f_S} \frac{1 + 4z^{-1} + z^{-2}}{1 - z^{-2}} \tag{16}$$

where $f_L(i)$ is the i-th estimated line frequency and f_S is the sampling frequency which is a fixed value of 8 kHz. $N_{ZC}(i)/N(i)$ is obtained by the CE.

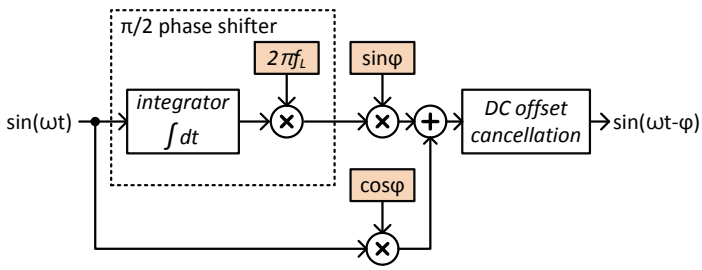

Fig. 5. Variable phase shifter

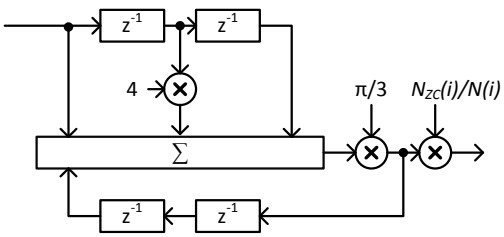

Fig. 6. Simpson integrator based π/2 phase shifter

The proposed CAL architecture consists of an arccosine block, a multiplier, a divider, adders, MUXs, registers, and a control block as shown in **Fig. 7**. The arccosine block is implemented using a coordinate rotation digital computer (CORDIC) algorithm [14], [15]. The multiplier and the divider are time-division multiplexed to calculate the calibration parameters such as the gains and delays. These parameters are stored in registers and then used for gain and phase compensations. The implementation results shows 27.15 % reduction in equivalent gate count compared with the coneventional CAL using individual arithmetic units. Details of the results are given in **Table 4**. The proposed calibration method can be performed only with a purely resistive load, which provides simplicity and convenience, although it has less accuracy compared with that using an accurate source. In addition, the calibration parameters such as the gain and phase are calculated in the built-in calibration engine, which decreases calibration time and simplifies calibration procedure.

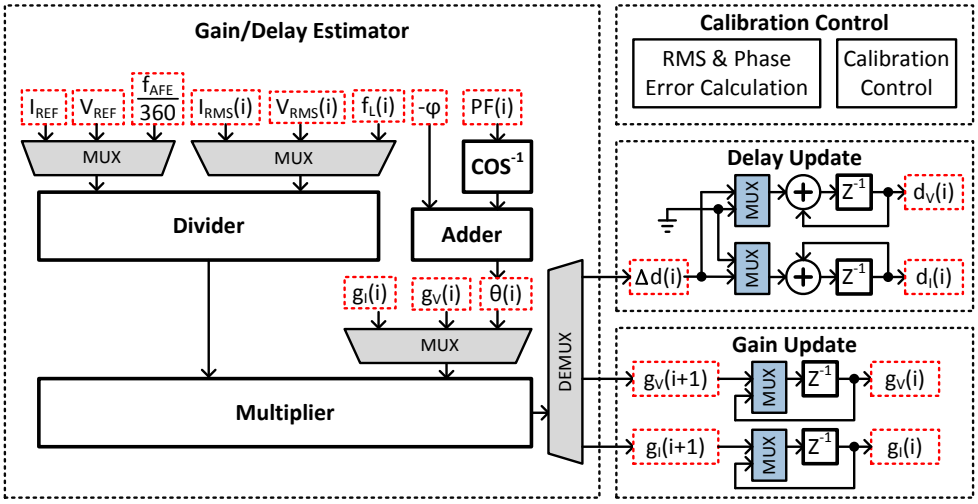

Fig. 7. Calibration engine architecture

Table 4. Comparison of conventional and proposed calibration engine

Function Blocks		Proposed		Conventional	
		Num.	Gate[1]	Num.	Gate
Gain/Delay Estimator	32-bit x 32-bit multiplier	1	2,185	3	6,555
	52-bit x 32-bit divider	1	926	3	2,778
	Arccosine block	1	5,311	1	5,311
	32-bit adder	1	216	1	216
	Temporary registers	1	266	0	0
	MUXs & etc.	1	545	0	0
Gain/Delay Update	Registers	1	478	1	478
	12-bit adder	2	162	2	162
	MUXs & etc.	1	418	1	418
Calibration Control	Error calculation & control	1	2,227	1	2,227
	Debugging logics & etc.	1	1,782	1	1,782
Total gate count			14,516		19,927

[1]Gate refers to a 2-input NAND gate

4. Implementation Results and Performance Analysis

4.1 Implementation Results

The chip micrograph is shown in **Fig. 8**. The chip is fabricated with 0.18-μm six-layer metal CMOS process and housed in a 32-pin QFN package. It operates at a clock speed of 4096 kHz, and consumes 9.84 mW in 3.3 V supply. The implementation details and results are given in **Table 5**. The proposed energy metering chips is composed of an AFE and a digital block. The AFE is implemented with two PGAs, two ΣΔ modulators, and a low-dropout (LDO) regulator. The digital block includes a filter block, a CE, a CAL, internal registers, a UART, an I2C, and a SPI. The total gate count is 135 k. The gate count ratios of the CE and the CAL are 15.1 % and 10.7 % of the whole gate count, respectively. **Table 6** shows the implementation details for the digital block.

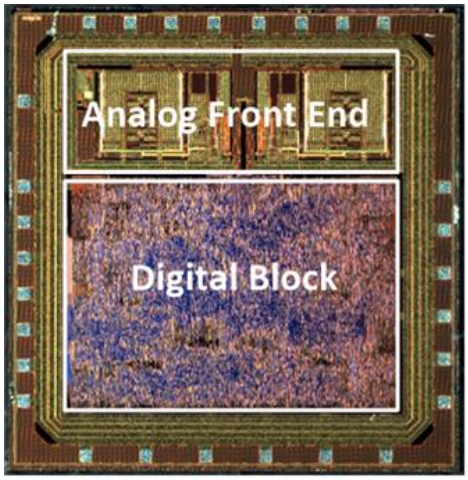

Fig. 8. Chip micrograph

Table 5. Implementation results for energy metering chip

Parameter	Value
Technology	0.18-μm six-layer metal CMOS
Die Size (mm^2)	2.310 x 2.340
Clock Rate (kHz)	4096
Supply Voltage (V)	3.3
Power Consumption (mW)	9.84 (core: 1.06, I/O: 0.04, analog: 8.74)
Package	32-pin QFN

Table 6. Implementation results for digital block

Digital Blocks	Equivalent Gates[1] (k)	Ratio (%)
Filter & Compensation	64.1	47.5
Computation Engine	20.3	15.1
Calibration Engine	14.5	10.7
Registers & External I/F	36.1	26.7
Total	135	100.0

[1]Equivalent Gate refers to a 2-input NAND gate

A signal-phase energy meter is implemented using the proposed chip as shown in **Fig. 9**. It consists of a CT, a voltage transformer (VT), the proposed energy metering chip, a switched mode power supply (SMPS), a regulator, and an 8-pin connector. The CT and the VT are used as the current and the voltage sensors, respectively. The SMPS and the regulator are used to generate 3.3 V supply. The chip communicates with an external Wi-Fi module through the 8-pin connector. To verify the functionality and reliability of the proposed energy metering chip, it is tested in the laboratory as shown in **Fig. 10**. The energy meter measures 220 V AC voltage and current applied to the loads, which are two 100 W and a 30 W light bulbs, and calculates the corresponding electric qualities. The values calculated from the energy meter are transported to the monitoring computer via Wi-Fi. The proposed energy metering chip was showed successful operation.

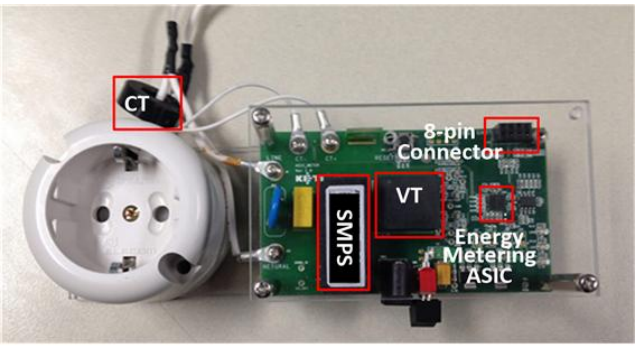

Fig. 9. Implementation of the energy meter using the proposed chip

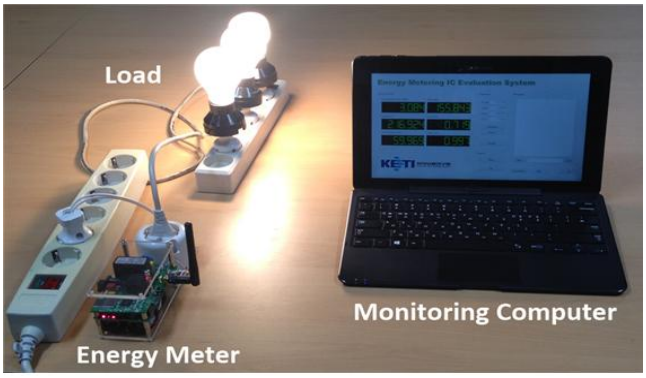

Fig. 10. Test environment for the proposed energy metering chip

4.2 Performance Analysis

Simulations are performed to demonstrate the effectiveness of the proposed phase calibration scheme using the variable phase shifter. A 60 Hz frequency voltage and current signal is generated. The phase difference between the voltage and current is included. The voltage and current are sampled at 8 kHz. Taking the signal values sampled at 8 kHz for 1 second, the phase difference between the voltage and current is estimated using (9). **Fig. 11** shows an absolute value of estimated phase errors (EPEs) at 0.1, 0.5, 1.0, and 2.0 phase differences (PDs) between the voltage and current. In this figure, solid lines and dashed lines denote the EPE performances of the conventional and proposed schemes as a function of the SNRs, respectively. The proposed scheme uses the variable phase shifter to rotate the phase of the voltage to 60 ˚. The EPE of the proposed scheme slightly increases with low SNR regardless of

PD while the EPE of the conventional scheme dramatically increases in less than 70 dB SNR at low PD. Thus, the proposed scheme is less sensitive to PD and noise. The conventional scheme becomes more sensitive to noise as PD to be estimated becomes smaller.

To verify the accuracy of the proposed energy metering chip, relative errors of the current RMS, active power, and reactive power are measured. The relative error is defined by

$$e_{\%} = \frac{N_2 - N_1}{N_1} \times 100 \tag{17}$$

where N_1 is the reference value and N_2 is the measured value. The measurement accuracy is tested on the energy metering chip calibrated with the proposed gain and phase calibration scheme. A programmable signal generator is used to supply the energy metering chip with known voltages and currents at various power factors. The signal generator creates 2 signals: a 60 Hz sine wave for the voltage channel and a 60 Hz sine wave for the current channel. The relative error for the current RMS, active power, and reactive power measured by the energy metering chip is calculated by varying the size of the sine wave for the current channel. **Fig. 12** shows the measured relative error of the current RMS. The measured error is less 0.1% over a 2000:1 dynamic range. The measured relative error of the active power is shown in **Fig. 13**. The solid line represents the relative error at a power factor of 1 and the measured error is less 0.1% over a 2000:1 dynamic range. The dash-dot and dashed lines show errors at lagging and leading power factors of 0.5, respectively. The measured errors are less 0.1% over a 1000:1 dynamic range and within 0.2% over a 2000:1 dynamic range. **Fig. 14** shows the measured error of the reactive power. The solid line indicates the relative error at a power factor of 0. The dash-dot and dashed lines show errors at lagging and leading power factors of 0.87, respectively. The measured errors are less 0.1% over a 2000:1 dynamic range. **Fig. 15** and **Fig. 16** show the measured power spectral density and the measured signal-to-noise and distortion ratio (SNDR) of the ΣΔ modulator, respectively. The ΣΔ modulator achieves signal-to-noise ratio (SNR) of 88 dB and peak SNDR of 78 dB. Measurement results show that the proposed energy metering chip guarantees 0.1% measurement error precision for the current RMS, active power, and reactive power in current dynamic range of 1000:1. The wide current dynamic range allows a large variety of choices for the current sensor that interfaces with the chip, allowing simplification of the interface circuit.

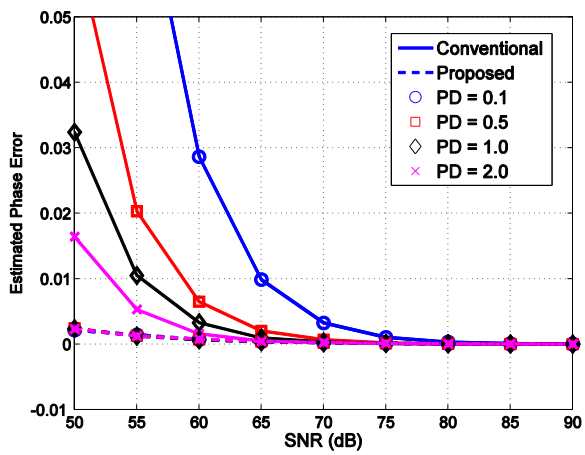

Fig. 11. Simulated phase error at various phase differences

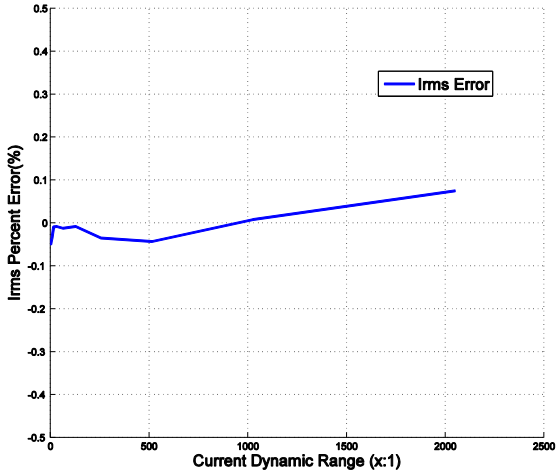

Fig. 12. Measured current RMS accuracy

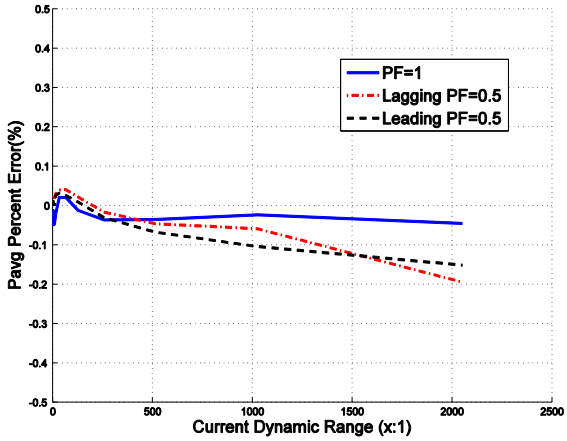

Fig. 13. Measured active power accuracy

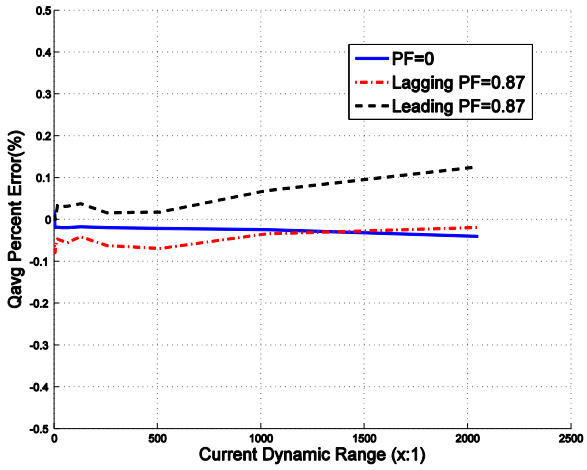

Fig. 14. Measured reactive power accuracy

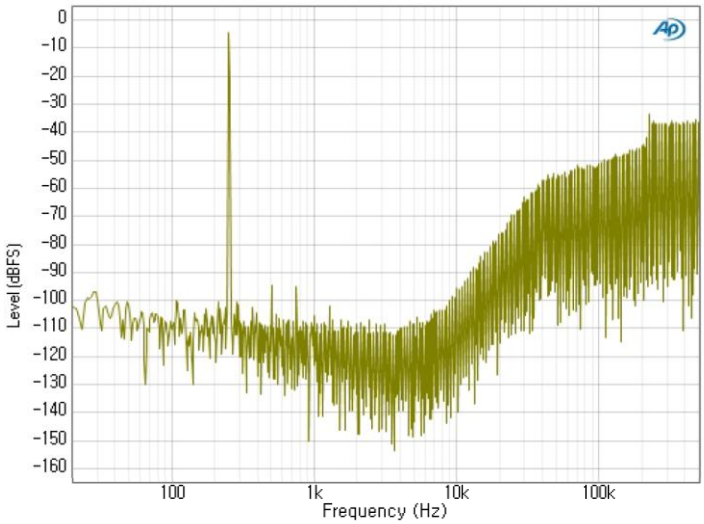

Fig. 15. Measured power spectral density

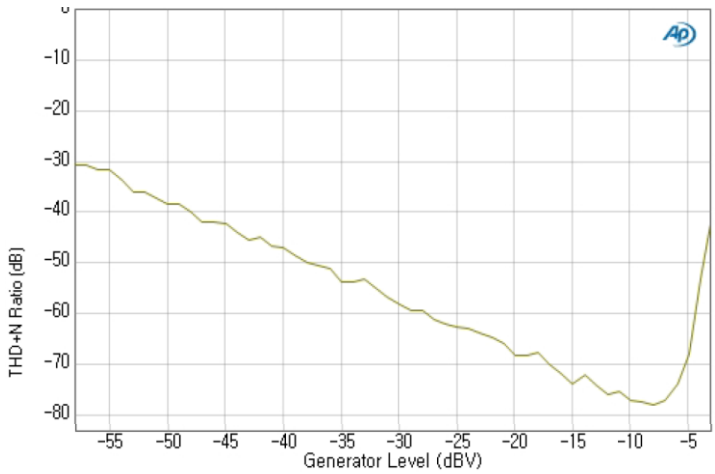

Fig. 16. Measured SNDR

5. Conclusion

In this paper, a single-phase energy metering chip with built-in calibration function was proposed. The proposed energy metering chip is fully implemented in hardwired logic and simplifies the computation engine using time-division multiplexed arithmetic units. In addition, it provides a simple and fast calibration scheme by using integrated digital calibration functionality. The chip was fabricated with 0.18-μm six-layer metal CMOS process and packaged in a 32-pin QFN package. It operates at a clock speed of 4096 kHz and consumes 9.84 mW in 3.3 V supply. Complexity analysis results show that the proposed computation engine and calibration engine achieved 33.99% and 27.15% reduction in equivalent gate count, respectively, compared to the computation engine and calibration engine that use individual arithmetic units. In addition, measurement results show that the relative errors of the current RMS, active power, and reactive power are less than 0.1% over a 1000:1 current dynamic range. As a future work, efforts will be made in hardware

implementation cost reduction by merging the calibration engine into the computation engine using time-division multiplexed arithmetic units. In addition, the performance of sigma-delta modulator and PGA needs to be improved to secure the energy metering chip's precision and wide current dynamic range.

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